PTM

PRIMARIUS

Power Device Design Verification

Introduction

PTM is a suite of tools to enhance the design analysis of power devices and power chip. It can extract Rdson with high precision and verify the devices' switching behavior, ensuring reliability and lifespan of IC products, which has been recognized and adopted by leading IDMs and Fabless companies.

Utilizing a proprietary edge-based 3D mesher and 64-bit numerical solvers, PTM excels in optimizing Rdson and gate delay in power transistor arrays. The suite provides detailed insights into current distributions, electro-migration rule violations, and layout analyses, allowing designers to pinpoint potential issues. Designers have full control over terminal placement and excitation, supported by test benches with Voltage Controlled Voltage Source (VCVS) for high-precision sense device design. PTM's co-design capability extends to power device die, package, and PCB, ensuring an optimal thermal performance and avoiding over-design or costly packaging solutions. The suite's integrated environment combines a state-of-the-art 3D solver with a user-friendly results viewer, offering cross-linked reports and field views for a comprehensive understanding of simulation outcomes.

With a focus on precision and efficiency, PTM offers unique advantages in its utilization of cutting-edge technology and an integrated environment. The proprietary edge-based 3D mesher and 64-bit numerical solvers set PTM apart, enabling accurate simulations and optimizations. Beyond its technical capabilities, PTM stands out for its co-design capability, allowing designers to harmonize power device die, package, and PCB for optimal thermal performance. This not only meets thermal requirements effectively but also prevents over-design and the need for expensive packaging solutions. The suite's layout analysis and visualization features provide a detailed view of current densities and electro-migration rule violations. Designers can focus on potential trouble spots by adjusting mesh density for enhanced accuracy. PTM's user-friendly results viewer with cross-linked reports and field views completes its integrated environment, ensuring a seamless and insightful design process for power devices in demanding applications.

Rdson
- 3D all-angle mesh solver
- Extract & optimize Rdson
- Identify current crowding, EM & IR drop issues on layout

Gate Delay
- Model propagation delay
- Optimize turn-on/turn-off
- Simulate power device gate net layout

Electro-Thermal
- True 3D simulation accuracy with advanced sparse matrix iterative solvers
- Static & transient ET simulation
- Analyze thermal effects & reliability

Key Advantages

Accurate
- Extract & optimize Rdson with high precision

Efficient
- Simulates and verifies electro-migration problems, IR-drops,and gate delay in the device

High–capacity
- Very large capacity & simulation speed

Powerful
- Ensure reliability and life time specifications

Advanced
- Advanced structure based “all-angle” mesher & highly accurate 3D field solver technology

Integrated
- Co-design capability for power device die, package and PCB

User–friendly
- Easy to set up and to use

Applications

- AMS Power Device Design
- Automotive Power Device Design
- PMIC Switching Power Supplies Power Device Design
- DC-DC Converters Power Device Design
- High Voltage Switches Power Device Design
- Large Digital Chips for On-chip Power Management Optimization
- Co-design of Power Device Die/Package/PCB

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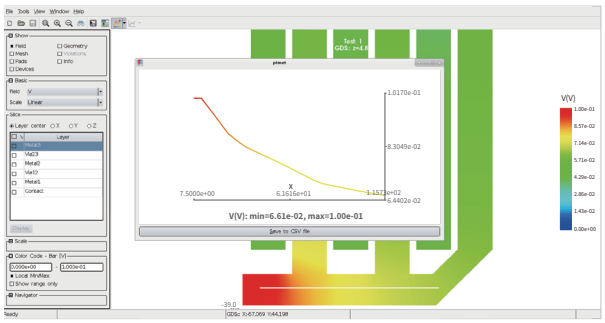
Specifications

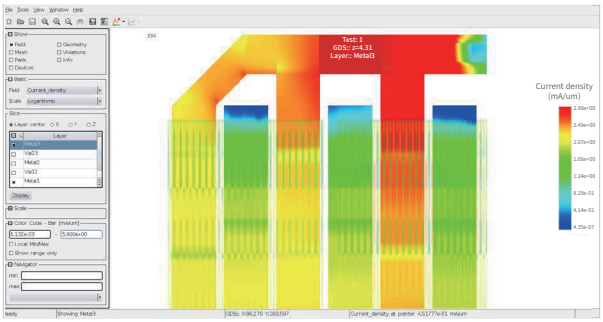
- Rdson
  - Simulates power device layout and allows to lower Rdson
  - Ensure reliability with Current Density / electro-migration checks
- Gate Delay
  - Models propagation delays in the gate net of power transistors
  - A distributed model of the gate net is used
  - Resistances in metal and poly lines are extracted
  - Capacitance of active area is modeled in a distributed fashion
  - Number of sections in the distributed model can be selected by the user
- Electro-Thermal
  - Chip/package-level 3D electro-thermal coupling and reliability analysis
  - Computes dynamic currents and Joule self-heating in metal & active area
  - Models heat flow in chip & package
  - Supports thermal planning
  - Supports non-linear temperature-dependent models
  - Self-consistent solution of electrical and thermal equations in 3D solver
  - Silicon verified accuracy
  - Imports GDSII

Application Examples

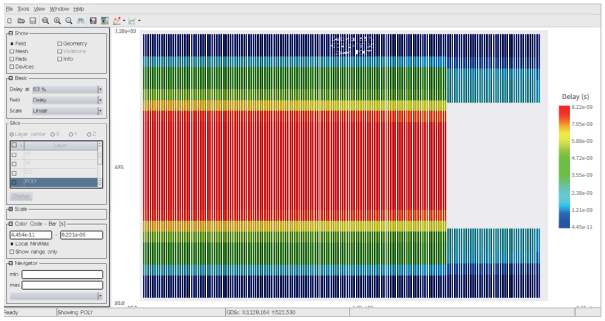
IR Drop/Voltage Analysis



Current Density Analysis



Gate Delay Analysis



Electro-Thermal Analysis