LibWiz

PRIMARIUS

Standard Cell Library Validation Solution

Introduction

As the semiconductor process technology node continues to scale, standard cell library providers face challenges associated with ever-increasing library complexity, as driven by the chip design process. Consistency and validity of heterogeneous cell libraries must be guaranteed to eliminate unnecessary design schedule delays. LibWiz provides a solution for trend analysis between PVT corners to ensure library integrity. Based on these analysis results, LibWiz also supports datasheet generation for use by chip designers. In addition, LibWiz supports seamless abstract layout generation from full-custom physical layout design effectively. The standard cell library is specified as Verilog HDL, OASIS (GDS-II), SPICE, Liberty, and LEF. So, it is essential to keep the consistency of all views. LibWiz utilizes a cross-check methodology to extract common parameters in each cell library and then checks consistency between libraries. LibWiz checks formal syntax and semantics of all libraries and supports a sequential process to check function equivalence and all properties such as cell area, pin list, pin property as direction, and timing arcs. LibWiz features a user-friendly GUI environment with cross-probing functions and generates HTML, PDF, and TXT format files for convenient analysis and post-processing of data.

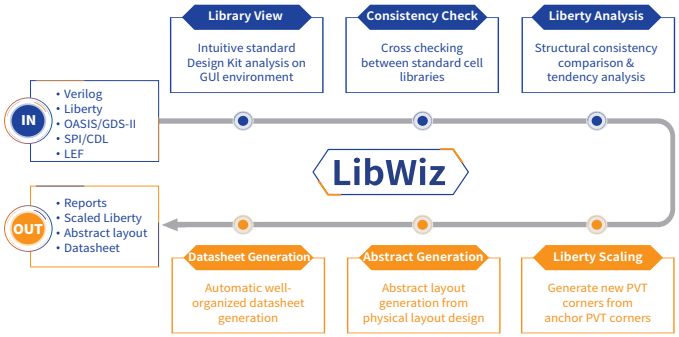
- Guarantee consistency between cell libraries
- Automate datasheet generation
- Achieve integrity of Liberty library
- Generate cell abstraction from physical layout

Key Advantages

- Achieve integrity of Liberty library
- Automatic datasheet generation
- Prevent inconsistency between library views
- Convenient cell abstract generation from physical layout

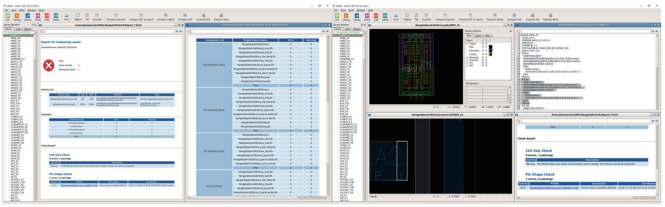
Specifications

- Library view
- Consistency check
- Liberty analysis
- Liberty scaling
- Abstract generation
- Datasheet generation

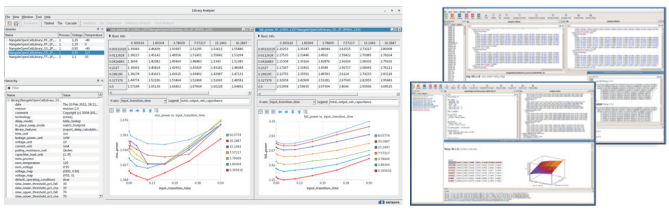


Application Examples

Consistency check between cell libraries



Liberty library analysis



Applications

- Standard cell & IO library design
- Analog/Mixed-signal IP & full custom layout design

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