NanoSpice SI

PRIMARIUS

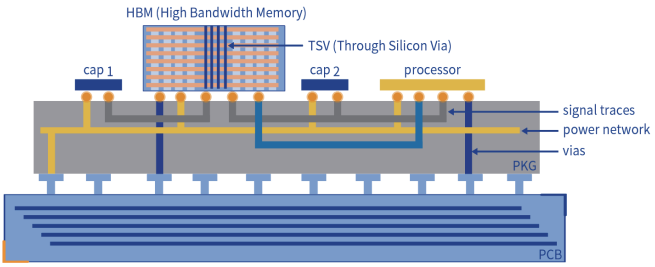
NanoSpice Signal Integrity Solution

Introduction

NanoSpice SI is a fast and precise signal integrity solution dealing with jitter, crosstalk, ringing, ground bounce, and noise problems brought by tighter packaging space and increasing clock frequencies.

With extensive SI models and analysis support, designers can accurately and quickly predict signal integrity issues under such conditions.

Signal Integrity Design on Chip, Package, and PCB Level

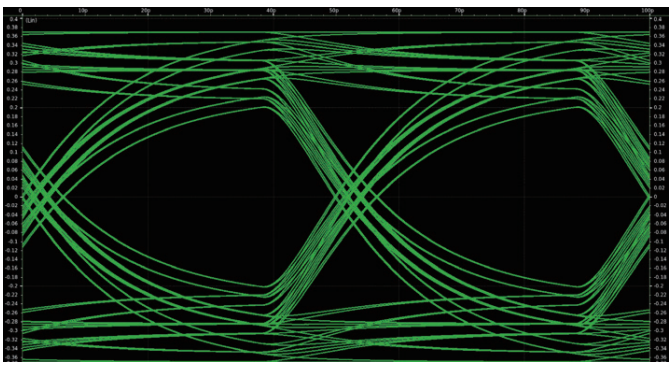


Key Advantages

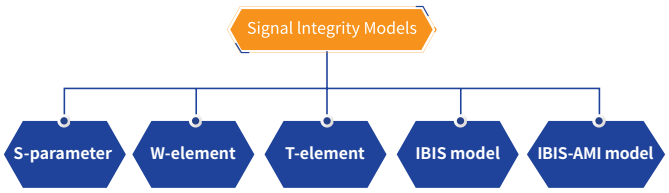
- Extensive model and element support for SI simulation
- Support S-parameters with up to a thousand ports and proven time-domain accuracy
- Superior simulation performance

Applications

- Chip-package co-simulation
- Package-Board-PDN network co-simulation of memory chips
- Noise/Jitter/Crosstalk analysis of high-speed serial interfaces



Typical device models for Signal Integrity



Specifications

- S-parameter analysis
  - To extract small-signal S-parameters for a general multi-port network.
- Statistical eye analysis
  - High-speed serial interfaces
  - Evaluate eye diagrams and BER quickly and accurately
- AC/Tran analysis
- Transmission line models: W-element and T-element
- S-parameter models
- IBIS files and IBIS-AMI models

Application Examples

Testcase	Circuit Devices	Reference (s)	NanoSpice SI	Speedup
case1	210-port S-element IBIS element	79200	22042	3.59X
case2	210-port S-element IBIS element	183600	36026	5.10X
case3	210-port S-element IBIS element	3600	513	7.02X
case4	190-port S-element IBIS element	8108	2165	3.75X
case5	179-port S-element	8953	1817	4.93X
case6	728-port S-element IBIS element	138593	45161	3.07X
case7	36-port S-element	263	96	2.74X